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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,581	06/24/2003	Lyle E. Adams	63479.0109	1633

23309 7590 06/09/2004

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,581	ADAMS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030624*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 7, 10, 11, 12, 15, 16, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,513,089 to Hofmann et al. ("Hofmann") and US Patent Application Publication Number 2003/0115500 to Akrout et al. ("Akrout").

3. In reference to Claim 1, Hofmann teaches a processor core (See Figure 1: 'PPC405 CPU'); one or more peripherals (See Figure 1: 'I^2C', 'GPIO', and 'UART'); and a first internal bus that couples said processor core to said peripheral(s) and carries signals from signal initiators to signal targets (See Figure 1: 'On-Chip Peripheral Bus'). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline

stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 1, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

4. In reference to Claim 2, Hofmann and Akrout teach the limitations as applied to Claim 1 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1: 'DMA Controller'), and said apparatus further comprises: a memory subsystem (See Figure 1: 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller'); and a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals, and that said second internal bus carries signals from signal initiators to signal targets (See Figure 1 'Processor Local Bus'), Hofmann does not teach said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of

Akrout, resulting in the invention of Claim 2, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

5. In reference to Claim 5, Hofmann and Akrout teach the limitations as applied to Claim 2 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both buses to access a plurality of common devices (See Figure 1), and that each topology is a bused topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 5, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

6. In reference to Claim 6, Hofmann teaches a processor core (See Figure 1: 'PPC405 CPU'); one or more peripherals (See Figure 1: 'I^2C', 'GPIO', and 'UART'); and a first internal bus that couples said processor core to said peripheral(s) and carries signals from signal initiators to signal targets (See Figure 1: 'On-Chip Peripheral Bus'). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline

stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 6, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

7. In reference to Claim 7, Hofmann and Akrout teach the limitations as applied to Claim 6 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1: 'DMA Controller'), and said apparatus further comprises: a memory subsystem (See Figure 1: 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller'); and a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals, and that said second internal bus carries signals from signal initiators to signal targets (See Figure 1 'Processor Local Bus'), Hofmann does not teach said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of

Akrout, resulting in the invention of Claim 7, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

8. In reference to Claim 10, Hofmann and Akrout teach the limitations as applied to Claim 7 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both buses to access a plurality of common devices (See Figure 1), and that each topology is a bused topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 10, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

9. In reference to Claim 11, Hofmann teaches providing a processor core (See Figure 1: 'PPC405 CPU'); providing one or more peripherals (See Figure 1: 'I^2C', 'GPIO', and 'UART'); and coupling a first internal bus to said processor core and to said peripheral(s), said first internal bus carries signals from signal initiators to signal targets (See Figure 1: 'On-Chip Peripheral Bus'). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the

use of a bus that has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 11, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

10. In reference to Claim 12, Hofmann and Akrout teach the limitations as applied to Claim 11 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1: 'DMA Controller'), providing a memory subsystem (See Figure 1: 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller'); and coupling a second internal bus to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus carries signals from signal initiators to signal targets (See Figure 1 'Processor Local Bus'). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of

Akrout, resulting in the invention of Claim 12, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

11. In reference to Claim 15, Hofmann and Akrout teach the limitations as applied to Claim 12 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both buses to access a plurality of common devices (See Figure 1), and that each topology is a bused topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 15, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

12. In reference to Claim 16, Hofmann teaches providing a processor core (See Figure 1: 'PPC405 CPU'); providing one or more peripherals (See Figure 1: 'I^2C', 'GPIO', and 'UART'); and carrying signals from signal initiators to signal targets over a first internal bus that couples said processor core to said peripheral(s) (See Figure 1: 'On-Chip Peripheral Bus'). Hofmann does not teach that said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that

has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 16, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

13. In reference to Claim 17, Hofmann and Akrout teach the limitations as applied to Claim 16 above. Hofmann further teaches that said one or more peripherals further comprises one or more DMA-type peripherals (See Figure 1: 'DMA Controller'), providing a memory subsystem (See Figure 1: 'SDRAM Controller' and 'SRAM/ROM Peripheral Controller'); and carrying signals from signal initiators to signal targets over a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals (See Figure 1 'Processor Local Bus'). Hofmann does not teach that said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target. Akrout teaches the use of a bus that has an arbitrary number of pipeline stages between a signal initiator and a signal target (See Figure 4 and Page 3 Paragraph 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 17, because a pipelined bus beneficially

improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

14. In reference to Claim 20, Hofmann and Akrout teach the limitations as applied to Claim 17 above. Hofmann further teaches that the first internal bus and the second internal bus have an overlapping topology enabling both buses to access a plurality of common devices (See Figure 1), and that each topology is a bused topology (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the SOC device of Hofmann with the pipelined bus of Akrout, resulting in the invention of Claim 20, because a pipelined bus beneficially improves the speed (frequency) at which the bus may be operated (See Page 3 Paragraph 27 of Akrout).

15. Claims 3, 8, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann and Akrout as applied to Claims 1, 2, 6, 7, 11, 12, 16, and 17 above, and further in view of US Patent Numbers 6,493,407 to Sheafor et al. ("Sheafor"), US Patent Number 6,173,349 to Qureshi et al. ("Qureshi"), and US Patent Number 5,469,547 to Pawlowski et al. ("Pawlowski").

16. In reference to Claim 3, Hofmann and Akrout teach the limitations as applied to Claims 1 and 2 above. Hofmann and Akrout do not teach that signals are point-to-point

and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 3, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

17. In reference to Claim 8, Hofmann and Akrout teach the limitations as applied to Claims 6 and 7 above. Hofmann and Akrout do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3

and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 8, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

18. In reference to Claim 13, Hofmann and Akrout teach the limitations as applied to Claims 11 and 12 above. Hofmann and Akrout do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See

Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 13, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

19. In reference to Claim 18, Hofmann and Akrout teach the limitations as applied to Claims 16 and 17 above. Hofmann and Akrout do not teach that signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking. Sheafor teaches using registered signals on a bus (See Figures 2 and 3 and Column 5 Lines 24-53). Qureshi teaches the use of a point-to-point bus (See Column 1 Lines 16-30). Pawlowski teaches a signaling protocol that uses full handshaking (See Column 1 Lines 19-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the registered signals of Sheafor, the point-to-point bus of Qureshi, and the handshaking protocol of Pawlowski, resulting in the invention of Claim 18, because flip-flop interfaces are advantageous and serve to convert the unidirectional buses of the physical layer to the bi-directional bus arrangement (See Column 5 Lines 44-48 and Column 6 Lines 22-24 of Sheafor); because point-to-point buses have lower latency, minimal bus contention, and the ability to support multiple simultaneous data transfers (See Column 1 Lines 26-28 of Qureshi); and because handshaking allows an asynchronous communication protocol to be used, which provide very high speed transfers of information between I/O devices and host computers and do not rely on a central clock which can limit the bandwidth (See Column 1 Lines 19-28 of Pawlowski).

20. Claims 4, 9, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann and Akrout as applied to Claims 1, 2, 6, 7, 11, 12, 16, and 17 above, and further in view of US Patent Number 5,410,194 to Freidin et al. ("Freidin").

21. In reference to Claim 4, Hofmann and Akrout teach the limitations as applied to Claims 1 and 2 above. Hofmann and Akrout do not teach that said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router. Akrout teaches that said pipeline stages comprise latches (See Figure 4 and

Page 3 Paragraph 27). Freidin teaches the benefits of using a flip-flop instead of a latch (See Column 1 Lines 16-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the flip-flops of Freidin, resulting in the invention of Claim 4, because a flip-flop is edge triggered, as opposed to level triggered like a latch, and thus has the advantage of being able to move a data signal from input to output at a selected time (See Column 1 Lines 20-22 of Freidin).

22. In reference to Claim 9, Hofmann and Akrout teach the limitations as applied to Claims 6 and 7 above. Hofmann and Akrout do not teach that said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router. Akrout teaches that said pipeline stages comprise latches (See Figure 4 and Page 3 Paragraph 27). Freidin teaches the benefits of using a flip-flop instead of a latch (See Column 1 Lines 16-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the flip-flops of Freidin, resulting in the invention of Claim 9, because a flip-flop is edge triggered, as opposed to level triggered like a latch, and thus has the advantage of being able to move a data signal from input to output at a selected time (See Column 1 Lines 20-22 of Freidin).

23. In reference to Claim 14, Hofmann and Akrout teach the limitations as applied to Claims 11 and 12 above. Hofmann and Akrout do not teach that said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router. Akrout teaches that said pipeline stages comprise latches (See Figure 4 and Page 3 Paragraph 27). Freidin teaches the benefits of using a flip-flop instead of a latch (See Column 1 Lines 16-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the flip-flops of Freidin, resulting in the invention of Claim 14, because a flip-flop is edge triggered, as opposed to level triggered like a latch, and thus has the advantage of being able to move a data signal from input to output at a selected time (See Column 1 Lines 20-22 of Freidin).

24. In reference to Claim 19, Hofmann and Akrout teach the limitations as applied to Claims 16 and 17 above. Hofmann and Akrout do not teach that said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router. Akrout teaches that said pipeline stages comprise latches (See Figure 4 and Page 3 Paragraph 27). Freidin teaches the benefits of using a flip-flop instead of a latch (See Column 1 Lines 16-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Hofmann and Akrout with the flip-flops of Freidin, resulting in the invention of Claim 19, because a flip-flop is edge triggered, as

opposed to level triggered like a latch, and thus has the advantage of being able to move a data signal from input to output at a selected time (See Column 1 Lines 20-22 of Freidin).

Double Patenting

25. Applicant is advised that should Claims 1-5 be found allowable, Claims 6-10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
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TJC

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